MARKED-UP VERSION SHOWING CHANGES MADE

IN THE SUBSTITUTE SPECIFICATION:

On **Page 1,** please amend the third paragraph, covering lines 16-23, as follows:

The TCP is a package [structured] including a tape carrier having a plurality of conductive leads formed thereon in a repeated pattern, wherein a semiconductor chip is placed on or in the tape carrier with its electrode pads lamination-contacted with corresponding ones of the carrier leads for electrical interconnection therebetween, the semiconductor chip being sealed by a sealing resin material or the like.

On **Page 2,** please amend the second paragraph, covering lines 14-25, as follows:

Another TCP structure is also known which includes a specific frame structure, called a "stiffener" in the semiconductor device art. The stiffener is provided around a semiconductor chip with its back surface in contact with a heat release member known as [a] a "heat spreader." In this TCP, a tape carrier is mounted on the stiffener for providing a junction between one end of its lead and the semiconductor chip while simultaneously providing a bump electrode at the other end of such lead. In this case the resultant TCP structure suffers from an excessive increase in thickness, which would result in an inability to achieve the desired multilayer structures.

On **Page 21,** please amend the third paragraph, beginning on line 23 and bridging to page 22, line 6, as follows:

Those surface portions of leads 1c excluding such a bump underlayer pattern 1c1 and the surfaces of adhesive 1b are coated with the solder resist 1d. The solder [re] resist 1d is about 20 μm in thickness, by way of example. In the first illustrative embodiment, the coat layer of lead 1c is made of the solder resist 1d thereby enabling miniaturization of the diameter of a connection hole for exposure of the bump underlayer pattern 1c1.

On **Page 23,** please amend the first paragraph, covering lines 1-11, as follows:

In addition, the plural bonding pads 2b stated supra are disposed in a region near the longer sides on the principal surface of the semiconductor chip 2. The bonding pads 2b are the electrodes that are used for permitting outward extension of electrodes of the semiconductor integrated circuit discussed above toward the outside of the semiconductor chip 2, which are made for example of aluminum (Al) or Al alloys. Each bonding pad 2b has [[its]] an upper surface on which a corresponding one of the lead-connecting bump electrodes 2a is formed.

On **Page 30,** please amend the second paragraph, covering lines 6-14, as follows:

4) Effectuation of polishing the back surface of the semiconductor chip 2 by spin-etching techniques or the like makes it possible for the semiconductor

chip 2 to become [thinner] thinned down [at] to 20 to 30 μm, for example. In addition, it is also possible to smoothen the back surface of the semiconductor chip 2, which in turn enables the semiconductor chip 2 to offer an anti-crackable structure with enhanced robustness against any bending stress applied thereto.

IN THE CLAIMS:

1. (Thrice Amended) A semiconductor device including a semiconductor chip having a principal surface and a back surface, opposite to said principal surface, disposed in a device hole provided in a tape carrier including a base layer and a lead portion bonded thereto with one end of a lead of said lead portion [on said tape carrier] being electrically connected to an external terminal of said semiconductor chip, said semiconductor device being disposed in the device hole such that the principal surface thereof is facing in the same direction as the side of said base layer to which said lead portion is bonded, characterized in that [said back surface of] said semiconductor chip [is] has a reduced thickness defined by spin-etching [a surface opposite to] of said back surface to effect a thinning of said semiconductor chip [so that said semiconductor chip is less in] to a thickness less than that of said tape carrier, and that said thinned semiconductor chip is sealed, covering both the principal and back surfaces thereof, by a seal resin material [so that said principal surface and said back surface of said semiconductor chip are covered with said seal resin material] to achieve a thickness at the resin sealed location of said device equal to the combined thickness of the base layer and lead portion of said tape carrier.

5. (Twice Amended) The semiconductor device as recited in claim 1, characterized in that [a seal resin] an injection port for use in seal resin injection is [formed] provided at part of said tape carrier [thereby causing] to effect coupling of said device hole [to be coupled] to a gate of a metal mold structure used during formation of said seal resin.

7. (Twice Amended) The semiconductor device as recited in claim 5, characterized in that an electroplated metal layer is formed at part of a surface of said tape carrier in close proximity to said injection port [passage] for seal resin injection, the part being brought into contact with the seal resin during formation of said resin seal.